

MITSUBISHI LSTTLs
M74LS138P

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

DESCRIPTION

The M74LS138P is a semiconductor integrated circuit consisting of a 3-bit binary-octal decoder/demultiplexer with enable inputs.

FEATURES

- 3 classes of enable inputs
- 4 to 16 decoder/demultiplexer functions are provided without use of external components.
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

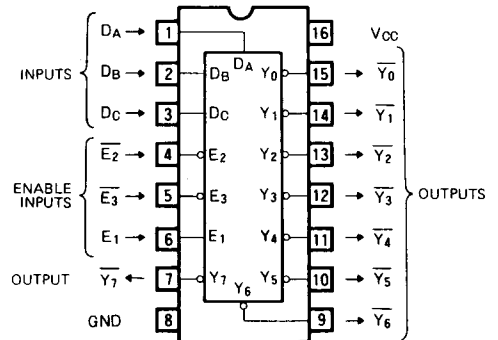
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

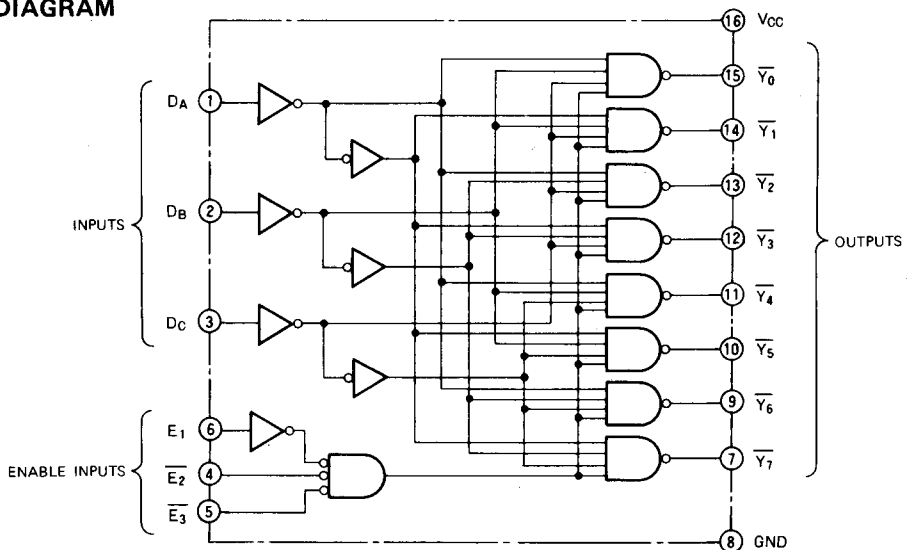
For use as a decoder, specify inputs D_A , D_B , and D_C in 3-bit binary code. In the case of decoding function, the E_1 is kept in high state while $\overline{E_2}$ and $\overline{E_3}$ are kept low. If E_1 , $\overline{E_2}$ and $\overline{E_3}$ are not in these conditions, all the outputs become high, irrespective of the status of $D_A \sim D_C$. For use as a demultiplexer, $\overline{E_1}$, $\overline{E_2}$ and E_3 are used as data inputs and D_A , D_B , and D_C as selection inputs. This forms a 1-line to 8-line demultiplexer.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

E ₁	\overline{E}_X	D _C	D _B	D _A	\overline{Y}_0	\overline{Y}_1	\overline{Y}_2	\overline{Y}_3	\overline{Y}_4	\overline{Y}_5	\overline{Y}_6	\overline{Y}_7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1: $\overline{E}_X = \overline{E}_2 + \overline{E}_3$
 X : irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5 ~ +7	V
V _I	Input voltage		-0.5 ~ +15	V
V _O	Output voltage	High-level state	-0.5 ~ V _{CC}	V
T _{opr}	Operating free-air ambient temperature range		-20 ~ +75	°C
T _{stg}	Storage temperature range		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit	
		Min	Typ	Max		
V _{CC}	Supply voltage	4.75	5	5.25	V	
I _{OH}	High-level output current	V _{OH} ≥ 2.7V		0	-400	μA
I _{OL}	Low-level output current	V _{OL} ≤ 0.4V		0	4	mA
		V _{OL} ≤ 0.5V		0	8	mA

ELECTRICAL CHARACTERISTICS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	V _{CC} = 4.75V, I _{IC} = -18mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = 4.75V, V _I = 0.8V V _I = 2V, I _{OH} = -400μA	2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = 4.75V	I _{OL} = 4mA	0.25	0.4	V
		V _I = 0.8V, V _I = 2V		I _{OL} = 8mA	0.35	0.5
I _{IH}	High-level input current	V _{CC} = 5.25V, V _I = 2.7V			20	μA
		V _{CC} = 5.25V, V _I = 10V			0.1	mA
I _{IL}	Low-level input current	V _{CC} = 5.25V, V _I = 0.4V			-0.4	mA
I _{OS}	Short-circuit output current (Note 2)	V _{CC} = 5.25V, V _O = 0V	-20		-100	mA
I _{CC}	Supply current	V _{CC} = 5.25V (Note 3)		6.3	10	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all output off-state.

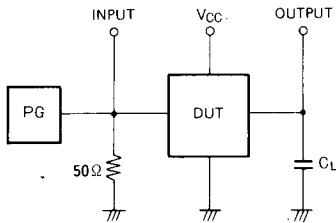
3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B, D_C to output $\bar{Y}_0-\bar{Y}_7$	delay gate stages 2	9	12	20	ns
t_{PHL}						
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs E_2, E_3 to outputs $\bar{Y}_0-\bar{Y}_7$	delay gate stages 3	16	14	27	ns
t_{PHL}						
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E_1 to outputs $\bar{Y}_0-\bar{Y}_7$	delay gate stages 2	10	15	18	ns
t_{PHL}						
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E_1 to outputs $\bar{Y}_0-\bar{Y}_7$	delay gate stages 3	8	15	26	ns
t_{PHL}						

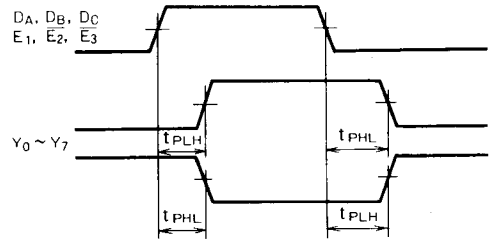
$C_L = 15 \text{ pF (Note 4)}$

Note 4: Measurement circuit



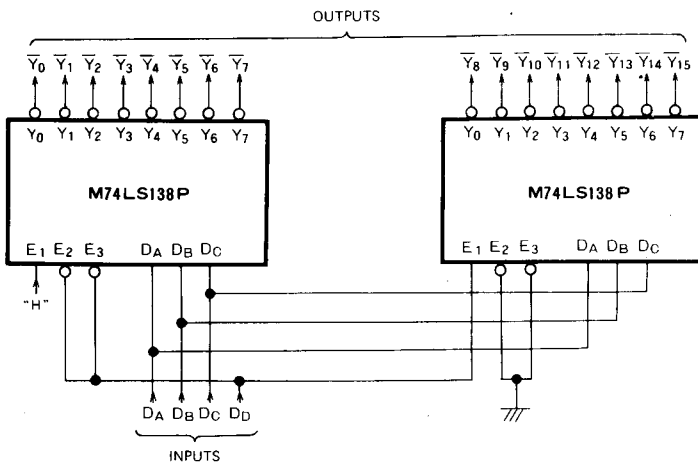
- (1) The pulse generator (PG) has the following characteristics:
 PRR = 1MHz, $t_r = 6\text{ns}$, $t_f = 6\text{ns}$, $t_w = 500\text{ns}$,
 $V_P = 3V_{pp}$, $Z_0 = 50\Omega$
- (2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

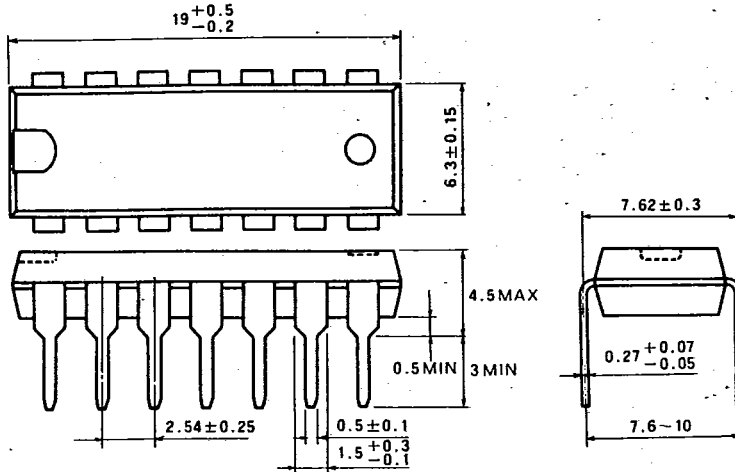
4-line to 16-line decoder/demultiplexer



T-90-20

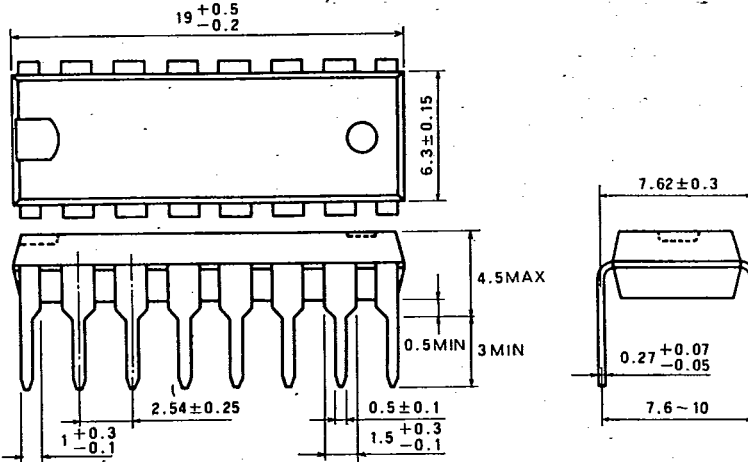
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

